UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/064,250	04/22/1998	ELIYAHOU HARARI	HARI.006USM	5711

36257 7590 11/02/2004

PARSONS HSUE & DE RUNTZ LLP
655 MONTGOMERY STREET
SUITE 1800
SAN FRANCISCO, CA 94111

EXAMINER	
LE, VU ANH	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 11/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/064,250	HARARI ET AL.	
	Examiner	Art Unit	
	Vu A. Le	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *63-73* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *69-73* is/are allowed.

6)☒ Claim(s) *63-68* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on *22 April 1998* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/22/98*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 63-65 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

2. Claims 63-65 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

3. The feature of "***flash control buffer means for performing data exchange between the flash memory and the interface means***" in claim 63 is not supported by the specification. Claim 63 claims "A semiconductor disk device, comprising:... flash control buffer means for performing data exchange between the flash memory and the interface means, ...". ***It means the flash buffer means is a part of the semiconductor***

disk device (33 of Fig.1B and Figs.6-8). However, the EEPROM array 33 (claimed as a semiconductor disk device in claim 63) in Fig.1B and Figs.6-8 does not show any "flash control buffer means". The Fig.1B depicts an interface 40 (claimed as "interface means"), a plurality of EEprom chips 43-47, and a logic and register circuit 57. The specification is also silent about the flash buffer means in the Eeprom array 33. Furthermore, in the Response to office action and request for interference received on Oct 27, 1998 (Paper No. 6) the applicant explains the receiver 313, FIFO 519 in Fig.6, FIFO 601 in Fig.7 and cache 705 in Fig.8 is the flash control buffer means. This explanation is incorrect since they are parts of controller circuit 31 and ***this controller circuit 31 is a separate circuit and is outside of the Eeprom array 33*** as shown in Fig.1B and Figs.6-8. The specification, page 17, lines 26-31 teach the memory device 33 (Eeprom array 33) is under the control of the controller 31 and the controller 31 is itself part of a microcomputer system under the control of a microprocessor. ***The receiver 313, FIFO 519 in Fig.6, FIFO 601 in Fig.7 and cache 705 in Fig.8 (explained as the flash control buffer means by the applicant) are parts of the controller 31 which is itself part of a micropcomputer system, so they are not parts of the Eeprom array 33.*** Thus, the semiconductor disk device as disclosed in the specification of the present application does not have the flash control buffer means. ***In short, a semiconductor disk device comprising a flash control buffer means as claimed in claims 63-65 is not supported by the specification.***

4. ***The feature of "access means for converting a sector address received from the external system into a substitute address and for accessing the flash memory according to the substitute address" is <u>not supported by the specification</u>*** since the access means for converting must be a part of the semiconductor disk device (Eeprom 33). However, Fig.1B and Figs.6-8 do not show the access means for converting. The specification and all figures do not say any about this access means for converting a sector address into a substitute address. Furthermore, in the Response to office action and request for interference received on Oct 27, 1998 (Paper No. 6) the applicant explains the access means for converting is supported by " Fig.1B, controller 31 and interface 40; Figs.2 & 3A, p.9, ln.10 through p.11, ln.6; Figs.6 & 7, p.17, ln.25 through p.24, ln.30". This explanation is incorrect. In Fig.1B, the controller 31 is outside of the Eeprom array 33, so controller is not considered as access means for converting and the interface 40 is "for exchanging data and addresses with an external system" as claimed in the claim 63, not "for converting a sector address received from the external system into a substitute address ...". The Fig.2 shows a plurality of sectors of flash Eeprom chips in Eeprom array 33 being selected by the controller 31 for erasing and Fig.3A illustrates a block diagram circuit 220 on a flash Eeprom chip. This block diagram circuit 220 has a decoder 233 for decoding the address, not converting the address (page 10, lines 9-11). Decoding an address is totally different from converting an address. For an example, an analog signal can be converted into a digital signal or a logical address can be converted into a physical address but an analog signal can NOT be converted into a digital signal or a

logical address can NOT be converted into a physical address. Page 10, lines 9-11 teach "address information is captured by an address register 231 and is decoded by an address decoder 233". Page 10, lines 13-15 teach "..., the controller sends the address of the sector 211 to the circuit 220. The address is decoded in line 235...". Fig.6 illustrates the read data path control. Page 17, lines 31-35 and page 18, lines 1-8 teach "To initiate the reading of a sector, the microprocessor loads a memory address generator 503 in the controller with a memory address for starting the read operation. This information is loaded through a microprocessor interface port 505. Then the microprocessor loads a DMA controller 507 with the starting location in buffer memory or bus address that the data read should be sent. Then the microprocessor loads the header information (Head, Cylinder and sector) into a holding register file 509. Finally, the microprocessor loads a command sequencer 511 with a read command before passing control to the controller 31." In order to read a data in the Eeprom array, a memory address must be loaded into a memory address generator and a header information such as head, cylinder and sector must be loaded into a holding register file. There is no address converting process here. Fig.7 illustrates the write data path. Page 20, lines 31-33 teach "The first portion of a write sequence is similar to a read sequence described previously." Since the first portion is the access process as described in the read process, so Fig.7 and page 17- page 24 do not teach the address converting process either.

5. ***Furthermore, the accessing to Eeprom array is controlled by the controller 33 and the microprocessor which are <u>outside</u> of the Eeprom array***. It

means the Eeprom array (a semiconductor disk device as claimed in claims 63-65) do not have access means for converting a sector address as claimed in claims 63-65. The present invention of this application is about redundant circuit to replace the defective memory cell or memory sector by a redundant memory cell or redundant memory sector. A mapping circuit is used to store defective address and replace the defective address by the redundant address when the defective address is access. ***When a non-defective address is accessed, there is no address replacement or no rerouting***. So the mapping circuit can not be considered as an access means for converting a sector address into a logical block address. The access means for converting a sector address into a logical block address converts ***all*** the sector address into a logical block address. ***In short, a semiconductor disk device comprising an access means for converting a sector address as claimed in claims 63-65 is not supported by the specification.***

7. With respect to claim 65, it claims "the substitute address includes a logical block address". This feature is not supported by the specification also. In the light of the specification, the substitute address is the ***spare address*** which is different from the ***logical block address***. ***The logical block address is the address for every block in the semiconductor disk device while the spare address is not the address of every block in the semiconductor disk device.***

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 66-68 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 66 recites "a data buffer connected to exchange data between the flash memory and the interface" which makes the scope of the claim indefinite. It is not clear what the data buffer connected to.

Allowable Subject Matter

5. Claims 69-73 are allowed.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vu A. Le whose telephone number is (571) 272-1871. The examiner can normally be reached on M-F (7:00-3:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vu A. Le
Primary Examiner
Art Unit 2824

10/29/04